Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 9 as with the following amended paragraph:

Cascaded converters, in which a first converter is controlled to generate a voltage or current, which serves as the source of input power for a DC-to-DC transformer stage, are known. A discussion of canonical forms of cascaded converters is given in Severns and Bloom, *ibid*, at, *e.g.*, pp. 114-117, 136-139. Baker, *ibid*, discusses the use of a voltage pre-regulator cascaded with a half-bridge, resonant, variable-frequency converter. Jones, U.S. Patent No. 4,533,986 shows a continuous-mode PWM boost converter cascaded with both PWM converters and FM resonant half-bridge converters for improving holdup time and improving the power factor presented to an AC input source. A zero-voltage transition, current-fed, full-bridge PWM converter, comprising a PWM boost converter delivering a controlled current to a PWM, full-bridge converter, is shown in Hua et al, "Novel Zero-Voltage Transition PWM Converters," IEEE Transactions on Power Electronics, Vol. 9, No. 2, March, 1994, p. 605. Stuart, U.S. Patent No. 4,853,832, shows a full-bridge series-resonant converter cascaded with a series-resonant DC-to-DC transformer stage for providing AC bus power to distributed rectified loads. A half-bridge PWM DC-to-DC transformer stage for use in providing input power to point-of-load DC-DC converters in a DPA is described in Mweene et al, **"A High-Efficiency 1.5 kW, 390-50V Half-Bridge Converter Operated at 100% Duty Ratio," APEC '92 Conference Proceedings, 1992, pp. 723-730** ~~*ibid*~~. Schlecht, U.S. Patent Nos. 5,999,417 and 6,222,742 shows DC-DC converters which incorporate a DC-to-DC transformer stage cascaded with a switching regulator. Vinciarelli, "Buck-Boost DC-DC Switching Power Conversion," U.S. Patent Application No. 10/214,859, filed August 8, 2002, assigned to the same assignee as this application and incorporated by reference, discloses a new, high efficiency, ZVS buck-boost converter topology and shows a front-end converter comprising the disclosed topology cascaded with a DC-DC converter and a DC-to-DC transformer.

Please replace the paragraph beginning at page 14, line 23 as with the following amended paragraph:

If the output voltage regulation requirement exceeds the resolution of an adaptive VTM array, finer regulation may be provided by an analog dissipative linear regulator in series with the input or output of a VTM array. ~~Figs.5A~~ **Figs. 5A** and 5B, show a linear regulator 107 in series with the output and input, respectively, of adaptive array 100. If, for example, an adaptive VTM array can achieve a regulation resolution of 1 percent with a manageable number of bits, the dissipation associated with using an appropriately designed analog series linear regulator, e.g. 107, to absorb substantially all of the 1% VTM array error may be negligible in terms of the overall converter efficiency. In fact such a loss may be smaller than the loss associated with a series-connected switching regulator (e.g., a "PRM", as described in the Factorized Application, and that may, in some applications, use the topology described in Vinciarelli, "Buck-Boost DC-DC Switching Power Conversion," U.S. Patent Application No. 10/214,859, filed Aug. 8, 2002, both assigned to the same assignee as this application and incorporated by reference). Use of a series linear regulator also eliminates the response delays and switching noise that would be introduced by use of a series-connected switching regulator. The analog series linear regulator also may provide enough bandwidth to effectively filter "hash" or "digital jitter" that may be generated due to instances of reconfiguration of the array.

Please replace the paragraph beginning at page 16, line 27 as with the following amended paragraph:

As described in conjunction with Figs. 1-2 and 7, the adaptive VTM array concept may be realized with a multiplicity of separate VTMs having independent isolation transformers and appropriate K factors, with each such VTM separately controlled to operate at a respective switching frequency. However, the Sine Amplitude Converter ("SAC") is particularly well suited for use in an integrated version of an adaptive VTM array. A full-bridge SAC of the type described in the Factorized Application is shown in Fig. 3. The SAC includes one primary circuit and one secondary circuit. The primary circuit comprises transformer primary winding

W_P, in series with resonant capacitance C_R, and resonant inductance L_R (which may have a low Q (where the term "low Q" has the meaning given in the Factorized Application with respect to transformers for use in a SAC) and may partially or entirely consist of the primary reflected leakage inductance of the transformer) driven by primary switches ~~S1, S2, S3, S4~~SW1, SW2, SW3, SW4. The switches ~~S1, S2, S3, S4~~SW1, SW2, SW3, SW4, are controlled by the switch controller to operate at near resonance with short energy recycling intervals to provide zero voltage switching. The output circuit, which includes the transformer secondary winding W_P, coupled to a rectifier circuit and a filter capacitor, supplies power to the load.

Please replace the paragraph beginning at page 17, line 11 as with the following amended paragraph:

Referring to Fig. 4, an integrated adaptive array 200 using the SAC topology is shown having a plurality of full-bridge SAC input cells 201, 202, 203, 204 coupled to a common SAC output cell 208. The input cells may be the same as the primary circuit of Fig. 3 with the addition of a bypass capacitor, *e.g.* capacitors 212 and 222, a series switch, *e.g.* series switches 211, 222, and a shunt switch, *e.g.* shunt switch 210, 220 for each cell. Also the primary windings W_{P1}, W_{P2}, W_{P3}, ...W_{Pm} may be part of one transformer 205 having a single secondary winding W_S coupled to the output circuit 208. The number of turns N_1, N_2, N_3, ... N_m in the primary windings may be selected to provide the appropriate transformation ratio for each cell. Using the K, 2K digital ladder example of Fig. 1, the integrated adaptive array SAC 200 could have five input cells having respectively 16 turns, 8 turns, 4 turns, 2 turns and 1 turn. A resonant switch controller 207 common to all of the cells may operate the primary **switches SW1-SW4** ~~switches S_1-S_4~~ of all of the cells (and the synchronous rectifiers in the output cells if used) in synchronism.

Please replace the paragraph beginning at page 19, line 29 as with the following amended paragraph:

One benefit of the complementary pair of input cells is that common-mode currents that would otherwise be capacitively coupled between primary windings, 331, 332, and secondary

winding, 333, as illustrated by the flow of current I_{CM} between primary 340 and secondary 342 grounds in Figure 8, will be reduced. In illustration, Figure 8 incorporates several representative parasitic capacitances, C_{P1} through C_{P4} 334 – 337. When switches SW2 and **SW3 are** ~~**SW3are**~~ opened, the rate-of-change of voltage across parasitic capacitors C_{P1} 334 and C_{P2} 335 will be positive and the rate-of-change of voltage across parasitic capacitors C_{P3} 336 and C_{P4} 337 will be negative and the net flow of current in the capacitors will tend to cancel. Likewise, the currents in the parasitic capacitors will also tend to cancel when switches SW1 and SW4 are opened. The net common-mode current, I_{CM}, flowing between the primary and secondary side of the array can be reduced using this arrangement.

Amendments to the Drawings:

The attached 8 sheets of formal drawings include changes to Figs. 3, 4, and 6 and replaces the original sheets including Figs. 1-8.

In Figure 3, 4, and 6, reference designations S1, S2, S3, and S4 have been changed to SW1, SW2, SW3, and SW4 to correct duplicate use of reference designations.

Attachments following last page of this Amendment:

Formal Drawing Replacement Sheets (8 pages)
Annotated Sheets Showing Changes (3 pages)